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10/708,446	03/04/2004	CHIH-HSIANG YANG	11584-US-PA	2445

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
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EXAMINER	
PIZIALI, JEFFREY J	
ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
01/27/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/708,446	YANG, CHIH-HSIANG	
	Examiner	Art Unit	
	Jeff Piziali	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11 November 2008 has been entered.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. The drawings have not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the figures.

Specification

4. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 6-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. For example:

Claim 6 recites the subject matter: "*the differential input signal is amplified for a first predetermined period when the differential input signal changes from a high level to a low level, or from the low level to the high level, and the first predetermined period is less than a first period of the differential input signal being in a steady state*" (lines 7-10).

The Applicant points to Figure 7 as showing the above quoted subject matter (see Page 9 of the Amendment filed 11 November 2008). However, neither Figure 7 nor the corresponding portion of the specification describes predetermined periods, one period being less than any other period, amplification based on high/low level changes, or steady states.

Claim 7 recites the subject matter: "*the first differential signal amplifier, coupled to the first differential transmitter and triggered to amplify the differential input signal*

for the first predetermined period when the differential input signal changes from a high level to a low level, or from the low level to the high level" (lines 7-10).

Neither the specification nor the figures describes triggering to amplify the differential input signal for the first predetermined period when the differential input signal changes from a high level to a low level, or from the low level to the high level.

Claim 8 recites the subject matter: "*gates of the second and third transistors are coupled to a positive output end of the first differential receiver,... and gates of the first and fourth transistors are coupled to a negative output end of the first differential receiver*" (lines 7-12).

The Applicant points to Figure 5 as showing the above quoted subject matter (see Page 11 of the Amendment filed 11 November 2008). However, neither Figure 5 nor the corresponding portion of the specification describes transistor gates coupled to positive/negative output ends of the first differential receiver.

Claim 9 recites the subject matter: "*a second terminal of the first sensor switch and a second terminal of the third sensor switch are coupled to a first terminal of the first resistor, a positive out end of the first differential transmitter, and a positive output end of the first differential signal amplifier, a second terminal of the second sensor switch and a second terminal of the fourth sensor switch are coupled to the a first terminal of the second resistor, a negative out end of the first differential transmitter, and a negative output end of the first differential signal amplifier; wherein, the first, second, third, and fourth sensor switches are controlled by whether the input differential signal changes*

from the high level to the low level, or from the low level to the high level, or the input differential signal is in the steady state" (lines 10-19).

The Applicant points to Figures 7-8 as showing the above quoted subject matter (see Pages 11-12 of the Amendment filed 11 November 2008). However, neither Figures 7-8 nor the corresponding portion of the specification describes coupling positive/negative out ends of the first differential transmitter and positive/negative output ends of the first differential signal amplifier; nor switches being controlled by whether the input differential signal changes from the high level to the low level, or from the low level to the high level, or the input differential signal is in the steady state.

Claim 10 recites the subject matter: "*the first differential output signal is amplified for a second predetermined period when the first differential output signal changes from a high level to a low level, or from the low level to the high level, the second predetermined period is less than a second period of the first differential output signal being in the steady state*" (lines 6-9).

The Applicant points to Figure 2 as showing the above quoted subject matter (see Page 10 of the Amendment filed 11 November 2008). However, neither Figure 2 nor the corresponding portion of the specification describes predetermined periods, one period being less than any other period, amplification based on high/low level changes, or steady states.

7. Claims 6-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. For example:

Claim 6 recites the subject matter: "*the differential input signal is amplified for a first predetermined period when the differential input signal changes from a high level to a low level, or from the low level to the high level, and the first predetermined period is less than a first period of the differential input signal being in a steady state*" (lines 7-10).

The Applicant points to Figure 7 as showing the above quoted subject matter (see Page 9 of the Amendment filed 11 November 2008). However, neither Figure 7 nor the corresponding portion of the specification describes predetermined periods, one period being less than any other period, amplification based on high/low level changes, or steady states.

Claim 7 recites the subject matter: "*the first differential signal amplifier, coupled to the first differential transmitter and triggered to amplify the differential input signal for the first predetermined period when the differential input signal changes from a high level to a low level, or from the low level to the high level*" (lines 7-10).

Neither the specification nor the figures describes triggering to amplify the differential input signal for the first predetermined period when the differential input signal changes from a high level to a low level, or from the low level to the high level.

Claim 8 recites the subject matter: "*gates of the second and third transistors are coupled to a positive output end of the first differential receiver,... and gates of the first and fourth transistors are coupled to a negative output end of the first differential receiver*" (lines 7-12).

The Applicant points to Figure 5 as showing the above quoted subject matter (see Page 11 of the Amendment filed 11 November 2008). However, neither Figure 5 nor the corresponding portion of the specification describes transistor gates coupled to positive/negative output ends of the first differential receiver.

Claim 9 recites the subject matter: "*a second terminal of the first sensor switch and a second terminal of the third sensor switch are coupled to a first terminal of the first resistor, a positive out end of the first differential transmitter, and a positive output end of the first differential signal amplifier, a second terminal of the second sensor switch and a second terminal of the fourth sensor switch are coupled to the a first terminal of the second resistor, a negative out end of the first differential transmitter, and a negative output end of the first differential signal amplifier; wherein, the first, second, third, and fourth sensor switches are controlled by whether the input differential signal changes from the high level to the low level, or from the low level to the high level, or the input differential signal is in the steady state*" (lines 10-19).

The Applicant points to Figures 7-8 as showing the above quoted subject matter (see Pages 11-12 of the Amendment filed 11 November 2008). However, neither Figures 7-8 nor the corresponding portion of the specification describes coupling positive/negative out ends of the first differential transmitter and positive/negative output

ends of the first differential signal amplifier; nor switches being controlled by whether the input differential signal changes from the high level to the low level, or from the low level to the high level, or the input differential signal is in the steady state.

Claim 10 recites the subject matter: "*the first differential output signal is amplified for a second predetermined period when the first differential output signal changes from a high level to a low level, or from the low level to the high level, the second predetermined period is less than a second period of the first differential output signal being in the steady state*" (lines 6-9).

The Applicant points to Figure 2 as showing the above quoted subject matter (see Page 10 of the Amendment filed 11 November 2008). However, neither Figure 2 nor the corresponding portion of the specification describes predetermined periods, one period being less than any other period, amplification based on high/low level changes, or steady states.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 6-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. The term "***a cascade driving circuit, suitable for a liquid crystal display***" in claim 6 (line 1) is a relative term which renders the claim indefinite. The term "***suitable***" is not

defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. For example:

It would be unclear to one having ordinary skill in the art what structure or functionality is necessarily present in order to make or render "***a cascade driving circuit, suitable for a liquid crystal display***." What structure or functionality makes a "***a cascade driving circuit, unsuitable for a liquid crystal display***"?

11. Claim 6 is indefinite where it specifies "***a first predetermined period***" (line 7), since "***predetermined,***" here merely appears to mean "*determined beforehand.*" For example, see Joseph E. Seagram & Sons, Inc. V. Marzall, Comr. Pats., 84 USPQ 180 (Court of Appeals, District of Columbia).

12. The term "***a high level***" in claim 6 (line 8) is a relative term which renders the claim indefinite. The term "***high***" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. For example:

It would be unclear to one having ordinary skill in the art what precise degree of "*highness*" is intended to be required before "***a level***" constitutes "***a high level***."

13. The term "***a low level***" in claim 6 (line 8) is a relative term which renders the claim indefinite. The term "***low***" is not defined by the claim, the specification does not

provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. For example:

It would be unclear to one having ordinary skill in the art what precise degree of "*lowness*" is intended to be required before "***a level***" constitutes "***a low level***."

14. Claim 7 recites the limitation "***the first driving circuit***" (line 1). There is insufficient antecedent basis for this limitation in the claim. For example:

It would be unclear to one having ordinary skill in the art whether this limitation is intended to be identical to, or distinct from, the earlier claimed, "***a first driving circuit unit***" (claim 6, line 3).

15. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results due to the claimed subject matter "***a first differential transmitter***" (line 4) and "***a first differential transmitter***" (line 5). For example:

It would be unclear to one having ordinary skill in the art whether these limitations are intended to be identical to, or distinct from, one another.

An omitted structural cooperative relationship results due to the claimed subject matter "***a high level***" in claim 7 (line 9) and "***a low level***" in claim 7 (line 9). For example:

It would be unclear to one having ordinary skill in the art whether these limitations is intended to be identical to, or distinct from, the earlier claimed, "***a high level***" in claim 6 (line 8) and "***a low level***" in claim 6 (line 8) respectively.

16. Claim 7 recites the limitation "***the first differential transmitter***" (line 7). There is insufficient antecedent basis for this limitation in the claim.

17. The term "***a high level***" in claim 7 (line 9) is a relative term which renders the claim indefinite. The term "***high***" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. For example:

It would be unclear to one having ordinary skill in the art what precise degree of "*highness*" is intended to be required before "***a level***" constitutes "***a high level.***"

18. The term "***a low level***" in claim 7 (line 9) is a relative term which renders the claim indefinite. The term "***low***" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. For example:

It would be unclear to one having ordinary skill in the art what precise degree of "*lowness*" is intended to be required before "***a level***" constitutes "***a low level.***"

19. Claim 7 recites the limitation "***the low level***" (line 10). There is insufficient antecedent basis for this limitation in the claim.

20. Claim 7 recites the limitation "***the high level***" (line 10). There is insufficient antecedent basis for this limitation in the claim.

21. Claim 9 recites the limitation "***a second current source and a third current source***" (line 3). There is insufficient antecedent basis for this limitation in the claim. For example:

It would be unclear to one having ordinary skill in the art whether a "***first current source***" is intended to be claimed.

22. Claim 9 recites the limitation "***the input differential signal***" (line 18). There is insufficient antecedent basis for this limitation in the claim. For example:

It would be unclear to one having ordinary skill in the art whether this limitation is intended to be identical to, or distinct from, the earlier claimed, "***a differential input signal***" (claim 6, line 3).

23. Claim 10 recites the limitation "***the second driving circuit***" (line 3). There is insufficient antecedent basis for this limitation in the claim. For example:

It would be unclear to one having ordinary skill in the art whether this limitation is intended to be identical to, or distinct from, the earlier claimed, "***a second driving circuit unit***" (claim 6, line 5).

24. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results due to the claimed subject matter "***a second differential output signal***" (claim 10, line 3) and "***a second data signal***" (claim 6, line 6). For example:

It would be unclear to one having ordinary skill in the art whether these limitations are intended to be identical to, or distinct from, one another.

25. Claim 10 is indefinite where it specifies "***a second predetermined period***" (line 6), since "***predetermined***," here merely appears to mean "*determined beforehand*." For example, see Joseph E. Seagram & Sons, Inc. V. Marzall, Comr. Pats., 84 USPQ 180 (Court of Appeals, District of Columbia).

26. The term "***a high level***" in claim 10 (line 6) is a relative term which renders the claim indefinite. The term "***high***" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. For example:

It would be unclear to one having ordinary skill in the art what precise degree of "*highness*" is intended to be required before "***a level***" constitutes "***a high level***."

27. The term "***a low level***" in claim 10 (line 7) is a relative term which renders the claim indefinite. The term "***low***" is not defined by the claim, the specification does not

provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. For example:

It would be unclear to one having ordinary skill in the art what precise degree of "*lowness*" is intended to be required before "***a level***" constitutes "***a low level***."

28. Claim 10 recites the limitation "***the low level***" (line 7). There is insufficient antecedent basis for this limitation in the claim.

29. Claim 10 recites the limitation "***the high level***" (line 7). There is insufficient antecedent basis for this limitation in the claim.

30. Claim 10 recites the limitation "***a second period of the first differential output signal***" (line 8). There is insufficient antecedent basis for this limitation in the claim. For example:

It would be unclear to one having ordinary skill in the art whether a "***first period of the first differential output signal***" is intended to be claimed.

31. The remaining claims are rejected under 35 U.S.C. 112, second paragraph, as being dependent upon rejected base claims.

32. The claims are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

As a courtesy to the Applicant, the examiner has attempted to also make rejections over prior art -- based on the examiner's best guess interpretations of the invention that the Applicant is intending to claim.

However, the indefinite nature of the claimed subject matter naturally hinders the Office's ability to search and examine the application.

Any instantly distinguishing features and subject matter that the Applicant considers to be absent from the cited prior art is more than likely a result of the indefinite nature of the claims.

The Applicant is respectfully requested to correct the indefinite nature of the claims, which should going forward result in a more precise search and examination.

Claim Rejections - 35 USC § 103

33. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

34. Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Pai (US 2004/0075636 A1)*** in view of ***Sunohara (US 2003/0038771 A1)*** and ***Chow (US 6,836,149 B2)*** and ***Matsuura (US 5,619,169 A)***.

Regarding claim 6, ***Pai*** discloses a cascade driving circuit, suitable for a liquid crystal display [e.g., Fig. 3; 36], comprising:

a first driving circuit unit [e.g., Fig. 3; 34A], for receiving a differential input signal [e.g., Fig. 3; 32] and generating a first differential data signal [e.g., Fig. 3; S11-S1384] for driving the LCD, and a first differential output signal; and

a second driving circuit unit [e.g., Fig. 3; 34B], coupled to the first driving circuit unit, for receiving the first differential output signal and generating a second data signal [e.g., Fig. 3; S21-S2384] for driving the LCD;

wherein the differential input signal is amplified [e.g., Fig. 3; 346AB] for a first predetermined period when the differential input signal changes from a high level to a low level, or from the low level to the high level, and the first predetermined period is less than a first period of the differential input signal being in a steady state (see the entire document, including Paragraphs 17-20).

Should it be shown that Pai teaches differential input signal amplification with insufficient specificity:

Sunohara is incorporated as teaching converting [e.g., Fig. 7; 32] and amplifying [e.g., Fig. 7; 31] a differential signal [e.g., Fig. 7; d0-dn] between each stage [e.g., Fig. 7; 30] of plural cascaded driving circuit units [e.g., Fig. 8A; 30-1 to 30-6], wherein the amplification and conversion occurs before the differential signal is transmitted from a differential signal transmitter [e.g., Fig. 7; 32] to the next stage (see the entire document, including Pages 7-8, Paragraph 52); as disclosed in the instant application.

Chow is incorporated as teaching a differential signal transmitter [e.g., Fig. 4; 400] comprising: a current source [e.g., Fig. 4; 404], for providing current that is required by the differential signal transmitter; and a first transistor [e.g., Fig. 4; 406], a second transistor [e.g., Fig. 4; 408], a third transistor [e.g., Fig. 4; 410], and a fourth transistor [e.g., Fig. 4; 412], wherein a drain of the first transistor and a drain of the second transistor are coupled to the current source, a source of the first transistor is coupled to a drain of the third transistor where a first signal [e.g., Fig. 4; 416] is drawn, a source of the second transistor is coupled to a drain of the fourth transistor where a second signal [e.g., Fig. 4; 418] is drawn, sources of the third and the fourth transistors are coupled [e.g., Fig. 4; 422] to ground voltage [e.g., Fig. 4; gnd], and the first signal associated with the second signal is the differential signal (see the entire document, including Column 4, Lines 6-24); as disclosed in the instant application.

Matsuura is incorporated as teaching an amplifier [e.g., Fig. 1] comprising: a first current source [e.g., Fig. 1; 4a] and a second current source [e.g., Fig. 1; 4b]; a first resistor [e.g., Fig. 1; 3] and a second resistor [e.g., Fig. 1; 3'], a second terminal of the first resistor and a second terminal of the second resistor are coupled to ground voltage [e.g., Fig. 1; 5]; and a first sensor switch [e.g., Fig. 1; 2a], a second sensor switch [e.g., Fig. 1; 2a'], a third sensor switch [e.g., Fig. 1; 2b], and fourth sensor switch [e.g., Fig. 1; 2b'], a first terminal of the first sensor switch [e.g., Fig. 1; 2a] and a first terminal of the second sensor switch [e.g., Fig. 1; 2a'] are coupled to the first current source [e.g., Fig. 1; 4a], a first terminal of the third sensor switch [e.g., Fig. 1; 2b] and a first terminal of the fourth sensor switch [e.g., Fig. 1; 2b'] are coupled to the second current source [e.g., Fig.

1; 4b], a second terminal of the first sensor switch [e.g., Fig. 1; 2a] and a second terminal of the third sensor switch [e.g., Fig. 1; 2b] are coupled to a first terminal of the first resistor [e.g., Fig. 1; 3] where a first signal [e.g., Fig. 1; 6'] is drawn, a second terminal of the second sensor switch [e.g., Fig. 1; 2a'] and a second terminal of the fourth sensor [e.g., Fig. 1; 2b'] switch are coupled to the a first terminal of the second resistor [e.g., Fig. 1; 3'] where a second signal [e.g., Fig. 1; 6] is drawn, the first signal associated with the second signal is the differential signal that is amplified (see the entire document, including Column 4, Lines 45-58 and Column 6, Line 53 - Column 7, Line 5); as disclosed in the instant application.

Pai does not expressly disclose amplifying the differential signal between each stage of the cascaded driving circuit units.

However, ***Sunohara*** discloses converting [e.g., Fig. 7; 32] and amplifying [e.g., Fig. 7; 31] a differential signal [e.g., Fig. 7; d0-dn] between each stage [e.g., Fig. 7; 30] of plural cascaded driving circuit units [e.g., Fig. 8A; 30-1 to 30-6],

wherein the amplification and conversion occurs before the differential signal is transmitted from a differential signal transmitter [e.g., Fig. 7; 32] to the next stage (see the entire document, including Pages 7-8, Paragraph 52).

Pai and ***Sunohara*** are analogous art, because they are from the shared inventive field of cascaded differential signal transmitters and receivers for driving a liquid crystal display panel.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use ***Sunohara's*** differential signal amplification and conversion

technique between each stage of ***Pai's*** driving circuit units, so as to stably transmit data with high reliability (see the entire document, including ***Sunohara***: Page 8, Paragraph 54, Lines 8-14).

Neither ***Pai*** nor ***Sunohara*** expressly discloses manufacturing the differential transmitter with any particular kind of transistor structure.

Pai and ***Chow*** are analogous art, because they are from the shared inventive field of differential signal transmitters making use of reduced swing differential signaling and mini-low voltage differential signaling (see the entire document, including ***Pai***: Page 2, Paragraph 17, Lines 6-8 and ***Chow***: Column 2, Lines 35-37).

Pai, ***Sunohara***, and ***Chow*** are further analogous art, because they are from the shared inventive field of driving liquid crystal display panels.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use ***Chow's*** differential transmitter structure to make ***Pai's*** and ***Sunohara's*** combined differential transmitter within each driving circuit unit, so as to provide a standardized differential data transmission interface and pathway (see the entire document, including ***Chow***: Column 1, Lines 27-38).

Neither ***Pai*** nor ***Sunohara*** expressly discloses manufacturing an amplifier with any particular kind of transistor structure.

Pai, ***Sunohara***, and ***Matsuura*** are analogous art, because they are all from the shared inventive field of differential signal processing circuitry.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use ***Matsuura's*** differential amplifier structure with ***Sunohara*** and ***Pai's*** combined cascaded differentially-amplified driving circuitry, so as to provide a high speed amplitude variable type differential amplifier capable of having a large and variable range of output amplitude (see the entire document, including ***Matsuura***: Column 3, Lines 46-48).

The above art combination would result in the cascade driving circuit described in the instant application, and therefore would necessarily and obviously provide differential input signal amplification in the same fashion as instantly claimed.

Regarding claim 7, this claim is rejected by the reasoning applied in rejecting claim 6; furthermore, ***Pai*** discloses a first differential receiver [e.g., Fig. 3; 344A & 344B], for receiving the differential input signal and transmitting the differential input signal to a first differential transmitter [e.g., Fig. 3; 348A & 348B]

a first differential transmitter [e.g., Fig. 3; 348A & 348B], coupled to the first differential receiver, for transmitting the differential input signal to a first differential signal amplifier; and

the first differential signal amplifier, coupled to the first differential transmitter and triggered to amplify the differential input signal for the first predetermined period when the differential input signal changes from a high level to a low level, or from the low level to the high level (see the entire document, including Paragraphs 17-20).

Regarding claim 8, this claim is rejected by the reasoning applied in rejecting claim 6; furthermore, ***Chow*** discloses the first differential transmitter [e.g., Fig. 4; 400] comprises:

a first current source [e.g., Fig. 4; 404]; and

a first transistor [e.g., Fig. 4; 406], a second transistor [e.g., Fig. 4; 408], a third transistor [e.g., Fig. 4; 410], and a fourth transistor [e.g., Fig. 4; 412], wherein a drain of the first transistor and a drain of the second transistor are coupled to the first current source, a source of the first transistor is coupled to a drain of the third transistor and a negative input end of the first differential signal amplifier, gates of the second and third transistors are coupled to a positive output end of the first differential receiver, a source of the second transistor is coupled to a drain of the fourth transistor and a positive input end of the first differential signal amplifier, sources of the third and the fourth transistors are coupled [e.g., Fig. 4; 422] to a ground voltage [e.g., Fig. 4; gnd], and gates of the first and fourth transistors are coupled to a negative output end of the first differential receiver (see the entire document, including Column 4, Lines 6-24).

Regarding claim 9, this claim is rejected by the reasoning applied in rejecting claim 6; furthermore, ***Matsuura*** discloses the first differential signal amplifier [e.g., Fig. 1] comprises:

a second current source [e.g., Fig. 1; 4a] and a third current source [e.g., Fig. 1; 4b];

a first resistor [e.g., Fig. 1; 3] and a second resistor [e.g., Fig. 1; 3'], a second terminal of the first resistor and a second terminal of the second resistor are coupled to a ground voltage [e.g., Fig. 1; 5]; and

a first sensor switch [e.g., Fig. 1; 2a], a second sensor switch [e.g., Fig. 1; 2a'], a third sensor switch [e.g., Fig. 1; 2b], and fourth sensor switch [e.g., Fig. 1; 2b'], a first terminal of the first sensor switch and a first terminal of the second sensor switch are coupled to the second current source, a first terminal of the third sensor switch and a first terminal of the fourth sensor switch are coupled to the third current source, a second terminal of the first sensor switch and a second terminal of the third sensor switch are coupled to a first terminal of the first resistor, a positive out end of the first differential transmitter, and a positive output end of the first differential signal amplifier, a second terminal of the second sensor switch and a second terminal of the fourth sensor switch are coupled to the a first terminal of the second resistor, a negative out end of the first differential transmitter, and a negative output end of the first differential signal amplifier;

wherein, the first, second, third, and fourth sensor switches are controlled by whether the input differential signal changes from the high level to the low level, or from the low level to the high level, or the input differential signal is in the steady state (see the entire document, including Column 4, Lines 45-58 and Column 6, Line 53 - Column 7, Line 5).

Regarding claim 10, this claim is rejected by the reasoning applied in rejecting claim 6; furthermore, ***Pai*** discloses

a third driving circuit unit [e.g., Fig. 3; 34, where the cascade continues to the right of the display], coupled to the second driving circuit unit;

wherein the second driving circuit generates a second differential output signal [e.g., Fig. 3; S21-S2384], the third driving circuit unit receives the second differential output signal and generates a third data signal [e.g., Fig. 3; S] for driving the LCD; the first differential output signal is amplified for a second predetermined period when the first differential output signal changes from a high level to a low level, or from the low level to the high level, the second predetermined period is less than a second period of the first differential output signal being in the steady state (see the entire document, including Paragraphs 17-20).

Response to Arguments

35. Applicant's arguments filed 11 November 2008 have been fully considered but they are not persuasive.

Applicant's arguments with respect to claims 6-10 have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571)272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
15 January 2009